AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A processor, comprising:

a crypto system;

an alignment buffer to receive header data and ciphered data from the crypto system, the crypto system encrypting data to form ciphered data so that an intended receiver with a correct cryptographic key may decrypt the ciphered data; and

a switch fabric having a plurality of transmit buffer elements to receive data from the alignment buffer, wherein the alignment buffer provides data to the switch fabric in blocks having a predetermined size,

wherein the crypto system comprises a plurality of crypto unit processing contexts and the alignment buffer comprises a number of buffer elements equal to a number of processing contexts, and

wherein the plurality of processing contexts are configured to process at least one data packet at a time and to store cipher keys and algorithm context associated with processing the at least one data packet.

2. (Previously Presented) The processor according to claim 1, further including an interface to transmit data from the switch fabric.

3. (Previously Presented) The processor according to claim 2, wherein the interface includes a SPI4 type interface.

4. (Previously Presented) The processor according to claim 2, wherein the interface includes an NPSI interface.

5. (Previously Presented) The processor according to claim 1, wherein the crypto system includes first and second crypto units.

Claim 6 (Cancelled)

7. (Previously Presented) The processor according to claim 1, wherein the crypto system includes a plurality of cipher cores.

8. (Previously Presented) The processor according to claim 7, wherein the plurality of cipher cores correspond to a plurality of cipher algorithms.

Claims 9 to 20 (Cancelled)

21. (Previously Presented) A network switching device, comprising:

a processor disposed on an integrated circuit comprising:

a crypto system, the crypto system encrypting data to form ciphered data so that an intended receiver with a correct cryptographic key may decrypt the ciphered data, the crypto system comprises a plurality of crypto unit processing contexts and the alignment buffer comprises a number of buffer elements equal to a number of processing contexts;

an alignment buffer to receive header data and the ciphered data from the crypto system; and

a switch fabric interface unit having a plurality of transmit buffer elements to receive the ciphered data from the alignment buffer, wherein the alignment buffer provides the ciphered data to the switch fabric in blocks having a predetermined size,

wherein the plurality of processing contexts are configured to process at least one data packet at a time and to store cipher keys and algorithm context associated with processing the at least one data packet.

22. (Cancelled)

23. (Original) The device according to claim 21, wherein the crypto system includes a plurality of cipher cores,

wherein the plurality of cipher cores correspond to a plurality of cipher algorithms.

24. (Original) The device according to claim 21, wherein the device includes a router.

25. (Currently Amended) A network, comprising:

a network switching device including a processor disposed on an integrated circuit comprising:

a crypto system, the crypto system encrypting data to form ciphered data so that an intended receiver with a correct cryptographic key may decrypt the ciphered data;

an alignment buffer to receive header data and the ciphered data from the crypto system; and

a switch fabric interface unit having a plurality of transmit buffer elements to receive the ciphered data from the alignment buffer, wherein the alignment buffer provides the ciphered data to the switch fabric in blocks having a predetermined size,

wherein the crypto system comprises a plurality of crypto unit processing contexts and the alignment buffer comprises a number of buffer elements equal to a number of processing contexts, and

wherein the plurality of processing contexts are configured to process at least one data packet at a time and to store cipher keys and algorithm context associated with processing the at least one data packet.

Claim 26 (Cancelled)

27. (Currently Amended) The network according to claim 25 [[26]], wherein the crypto system includes a plurality of cipher cores.

28. (Original) The network according to claim 25, wherein the network switching device corresponds to a router.

29. (Previously Presented) The processor of claim 6 wherein the plurality of processing contexts are configured to allow latency of loading cryptographic key material and packet data to be hidden by pipelining loading of the packet data and the key material into a first portion of the plurality of processing contexts with processing of the packet data in a second portion of the plurality of processing contexts.